

**HIGH PERFORMANCE IMPLEMENTATION OF EXPONENT ADJUSTMENT  
IN A FLOATING POINT DESIGN**

**ABSTRACT**

A floating point unit (FPU) which generates a correction signal and an inverted leading zero signal.

5      Exponent logic, is configured to generate an exponent value, a first incremented exponent value, and a second incremented exponent value. Exponent adjust and rounding logic configured to receive the exponent value, the first incremented exponent value, and the second incremented exponent value. The exponent adjust and rounding logic is further configured to add the inverted leading zero signal to the first incremented exponent value and the second incremented exponent value, thereby producing an exponent output value, a first incremented exponent output value, and

10     a second incremented exponent output value. Either the exponent output value, the first incremented exponent output value, or the second exponent output value are then selected.

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